

ANSI/ESD STM5.1-2007

ESD Association Standard Test Method

ANSI/ESD STM5.1-2007

Revision of ANSI/ESD STM5.1-2001

*For Electrostatic Discharge
Sensitivity Testing –*

*Human Body Model (HBM)
Component Level*



*Electrostatic Discharge Association
7900 Turin Road, Bldg. 3
Rome, NY 13440*

*An American National Standard
Approved November 12, 2007*

***ESD Association Standard Test Method
for Electrostatic Discharge Sensitivity Testing –
Human Body Model (HBM)
Component Level***

ESD Association
Approved September 16, 2007



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Published by:

**Electrostatic Discharge Association
7900 Turin Road, Bldg. 3
Rome, NY 13440**

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Printed in the United States of America

ISBN: 1-58537-139-4

(This foreword is not part of ANSI/ESD STM5.1-2007)

FOREWORD

The ANSI/ESD STM5.1-2001 document has been reviewed and updated in 2006. The basic specifications in the document have not changed. A list of the edits made to this document is shown in Annex F, titled “ANSI/ESD STM5.1-2007 Revision History.”

The most significant changes to the document include new definitions of different measurement terms that define the HBM peak current, I_{ps}. A new definition for the “No Connect Pin” has been added and the requirements to HBM stress this family of pins has been removed. The other changes to the document include the requirement to verify the peak current waveform for each independent “pulse generation circuit,” slight edits to how I_{ps} peak current can be verified in Section 7.0, relaxation of the 2 ohm requirement to 3 ohm requirement for the bus resistance between like name power and/or ground supply pins, optional check for “trailing current pulse,” and another optional check for the “voltage before the pulse.”

The removal of the HBM stressing of the No Connect Pin was made because the HBM Work Group believes the existing HBM simulators cannot correctly test these pins. New research has shown that the testing of this type of pin is more difficult due to the interaction of the HBM simulator tester parasitics. Until a better test procedure can be defined, the Work Group believes the best option at this time is to stop HBM stressing the No Connect Pin.

This revision includes two new optional measurements that address newly discovered HBM test equipment parasitic artifacts. They include an optional check for a “trailing current pulse” and an optional check for the “voltage before the pulse.” Two recent HBM research papers have demonstrated that HBM sensitivity levels can be falsely classified due to the parasitic artifacts unintentionally built into the HBM simulators. Two new sections, Annex C and D, have been added so that the user can determine if their HBM simulator has these artifacts. Not all semiconductor components are sensitive to these tester artifacts, but the Work Group wanted the ESD user community to know that these artifacts exist and can potentially influence the HBM sensitivity levels of semiconductor components. If a user suspects that the tester artifacts are a factor, the best option to prove or disprove this affect is to repeat the exact fail pin HBM stress combination using a two-pin manual HBM simulator. If the failures cannot be reproduced using the non-relay type HBM simulator, then the HBM failures may be due to the relay matrix simulator tester artifacts. The ESD equipment manufactures have developed equipment repairs to fix some of the existing HBM simulators. The user is advised to contact their ESD equipment manufacturer for further information.

Historically, this document’s test procedures were derived from MIL-STD-883D and MIL-STD-STD-750 Notice A (see Annex E). As a living document, updates and changes will be made to this document as they are required.

This document was originally designated EOS/ESD S5.1-1991 and approved on June 6, 1991. ANSI/EOS/ESD 5.1-1993 was a revision of EOS/ESD S5.1-1991 and was approved on June 9, 1993. ESD STM5.1-1998 was a revision and redesignation of ANSI/EOS/ESD S5.1-1993 and was approved on February 8, 1998. ANSI/ESD STM5.1-2001 was a revision of ESD STM5.1-1998 and was approved on May 20, 2001. ANSI/ESD STM5.1-2007 is a revision of ANSI/ESD STM5.1-2001 and was approved by the ESD Association Standards Committee on September 16, 2007. All documents were prepared by the 5.1 Device Testing (HBM) Subcommittee.

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ESD Association Standard Test Method for Electrostatic Discharge Sensitivity Testing Human Body Model (HBM) – Component Level

1.0 SCOPE AND PURPOSE

1.1 Scope

This document establishes the procedure for testing, evaluating, and classifying the electrostatic discharge (ESD) sensitivity of components to the defined human body model (HBM).

1.1.1 Existing Data

Data previously generated with testers meeting all waveform criteria of this standard shall be considered valid test data.

1.2 Purpose

The purpose of this document is to establish a test method that will replicate HBM failures and provide reliable, repeatable results from tester to tester, regardless of component type. Repeatable data will allow accurate comparisons of HBM ESD sensitivity levels.

2.0 REFERENCED PUBLICATIONS

Unless otherwise specified, the following documents of the latest issue, revision or amendment form a part of this standard to the extent specified herein:

ESD ADV1.0, ESD Association Glossary of Terms¹

ANSI/ESD STM5.2, Machine Model – Component Level¹

3.0 DEFINITIONS

The following definitions are consistent with those in the ESD Association Glossary of Terms.

Component. An item such as a resistor, diode, transistor, integrated circuit or hybrid circuit.

Component failure. A condition in which a tested component does not meet one or more specified static or dynamic data sheet parameters.

Data sheet parameters. The static and dynamic component performance data supplied by the component manufacturer or user.

Discrete component. An elementary electronic device constructed as a single unit.

Dynamic parameters. Parameters measured with the component in an operating condition. These may include, but are not limited to full functionality, output rise and fall times under a specified load condition, and dynamic current consumption.

Electrostatic discharge sensitivity (ESDS). The ESD level that causes component failure.

ESD withstand voltage. The maximum ESD level that does not cause component failure.

Human body model (HBM) ESD. An ESD event meeting the waveform criteria specified in this standard, approximating the discharge from the fingertip of a typical human being.

Ips_{max}. The peak current maximum value is the highest current value measured. This value includes the overshoot or ringing components due to internal test simulator RLC parasitics. (See Figure 2A.)

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Ips. The peak current value is determined by the current at time t (max) on the linear extrapolation of the exponential current decay curve. The linear extrapolation should be based on the current waveform data over a 40 nanosecond period beginning at t_{max} . (See Figure 2A.)

Ir. The current waveform oscillation in the short circuit waveform is the peak-to-peak ringing that can occur within the first 100 ns of Ips_{max} (See Figure 2A and Table 5).

Machine model (MM) ESD. An ESD event meeting the criteria specified in the MM Standard Test Method STM 5.2.

New equipment. Any new or recently purchased HBM testers or simulator test equipment.

No connect pin. A package interconnect (pin or ball) that is not bonded to any bond pad.

Old equipment. Any used or older HBM testers or simulator test equipment.

Pulse generation circuit. The circuit network that produces a human body discharge current waveform.

Ringing. High frequency oscillation superimposed on the waveform.

Shorted I/O pin. This pin is any I/O pin that is metallurgically connected (< 1 ohm) on the chip or within the package to another IO pin (or set of I/O pins).

Static parameters. Parameters measured with the component in a non-operating condition. These may include, but are not limited to: input leakage current, input breakdown voltage, output high and low voltages, output drive current, and supply current.

Step stress test hardening. A component can withstand higher voltage stress levels after subjected to multiple gradually increasing ESD stress voltages, as compared to a component subjected to a single lower stress voltage. For example: a component may fail at 1000 volts if subjected to a single stress, but fail at 3000 volts if stressed incrementally from 250 volts.

Spurious current pulses. Small HBM shaped pulses that follow the main current pulse, and should be less than 15% of Ips_{max} .

t_{max} . The time when Ips is at its maximum value (Ips (max)). (See Figure 2A.)

Trailing current pulse. A current pulse that occurs much greater than 1 microsecond after the HBM current pulse has decayed. (See Annex C.)

Voltage before the HBM current pulse. A voltage occurring at the device under test (DUT) just prior to the generation of the HBM current pulse.

4.0 HBM ESDS COMPONENT CLASSIFICATIONS

ESD sensitive components are classified according to their HBM ESD withstand voltage, regardless of polarity. The HBM ESDS component classification levels are shown in Table 1.

Table 1. HBM ESDS Component Classification

Class	Voltage Range
0	< 250
1A	250 to < 500
1B	500 to < 1000
1C	1000 to < 2000
2	2000 to < 4000
3A	4000 to < 8000
3B	≥ 8000

5.0 REQUIRED EQUIPMENT

5.1 HBM ESD Tester

An acceptable ESD tester is composed of equipment meeting the requirements of this standard. A schematically represented ESD tester is illustrated in Figure 1 and produces current pulse waveforms that meet the waveform characteristics as specified in Figures 2A, 2B and 3.

5.2 Waveform Verification Equipment

Equipment capable of verifying the pulse waveforms defined in this standard test method includes, but is not limited to, an oscilloscope, two evaluation loads and a current transducer.

5.2.1 Oscilloscope requirements:

- a. Minimum sensitivity of 100 milliamperes per major division (typically 1 centimeter) when used in conjunction with the current transducer specified in Section 5.2.3.
- b. Minimum single shot bandwidth of 350 megahertz.
- c. Minimum writing rate of one major division per nanosecond.

5.2.2 Evaluation loads. Two evaluation loads are necessary to verify tester functionality:

- a. Load 1: A solid 18–24 AWG (0.83 to 0.21 mm² cross-section) tinned copper shorting wire as short as practicable to span the distance between the two farthest pins in the socket while passing through the current probe.
- b. Load 2: A 500 ohm, ± 1%, 1000 volt, low inductance, sputtered film resistor (Caddock Industries type MG 714 or equivalent).

5.2.3 Current transducer requirements:

- a. Minimum bandwidth of 350 megahertz.
- b. Peak pulse capability of 12 ampere.
- c. Rise time of less than 1 nanosecond.
- d. Capable of accepting a solid conductor of 1.5 millimeters in diameter.
- e. Provide an output voltage per milliamperes as required in Section 5.2.1.a. (Usually between 1 and 5 millivolts per milliamperes.)

A Tektronix CT-1 or equivalent with a maximum cable length of 1 meter meets these requirements.

6.0 EQUIPMENT AND WAVEFORM REQUIREMENTS

6.1 Equipment Calibration

All equipment used to evaluate the tester shall be calibrated in accordance with the manufacturer's recommendation. This includes the oscilloscope, current transducer and high voltage resistor load. Maximum time between calibrations is one year. Calibration shall be traceable to national standards, such as the National Institute of Standards and Technology (NIST) in the United States, or comparable international standards.

6.2 Tester Qualification and Requalification

HBM ESD tester initial qualification in accordance with Section 7 shall be performed as part of the acceptance testing when the ESD tester is delivered or first used.

Perform the HBM ESD tester requalification described in Section 7.1 in accordance with the manufacturer's recommendation. Maximum time between full requalification tests is one year. Perform tester verification in accordance with Section 7.3 following repairs or servicing that could affect the waveform. Use the highest pin count test fixture board with a positive clamp socket for the waveform verification. All other test fixture boards shall be checked routinely when they are used in accordance with Section 8.1.2.

NOTE 1: A positive clamp test socket is a zero insertion force (ZIF) socket with a clamping mechanism. It allows the shorting wire to be easily clamped into the socket. Examples are dual in-line package (DIP) and pin grid array (PGA) ZIF sockets.

6.3 Tester Waveform Records

6.3.1 Tester Waveform Records: New Equipment

Record positive and negative waveforms for both the short circuit and 500 ohm load resistor during the tester initial qualification procedures. Retain the waveform records until the next calibration or for the duration specified by the internal record keeping procedures. Test each socket in accordance with Section 7.1. Use the voltage levels defined in Section 7.2.

6.3.2 Tester Waveform Records: Old Equipment

Record positive and negative current waveforms using both the short circuit wire and the 500 ohm load resistor as defined in Section 7.1. Retain the waveform records until the next calibration or for the duration specified by the internal record keeping procedures. Use the highest pin count test fixture with a positive clamp socket. Perform these tests as recommended by the equipment manufacturer or during the yearly calibration cycle.

6.4 Trailing Current Pulse Check (Optional)

Some HBM simulators have been found to falsely classify HBM sensitivity levels due to the parasitic artifacts unintentionally built into the HBM simulators. To determine if the "Trailing Current Pulse" parasitic artifact is present, the following optional test equipment check has been developed. The maximum trailing current pulse level is defined as the maximum peak current level observed through a 10 kilohm test load (current = voltage across test load divided by 10 kilohm) after the normal ESD pulse(s). The time period, which shall be surveyed for after pulse leakage, is from 100 microseconds to 1 millisecond after the decay of ESD current pulse. In the case that a secondary current pulse is observed, begin the 100 microsecond measurement point from the start of the second pulse.

The magnitude of the trailing current pulse shall be less than 4 microamperes when the applied HBM stress voltage is at 4000 volts. This includes both positive and negative polarities.

See Annex C for the measurement setup procedure for detecting this type of pulse.

This trailing pulse check is optional for older design HBM simulators and is not a required test.

7.0 QUALIFICATION AND VERIFICATION PROCEDURES

7.1 HBM ESD Tester and Test Fixture Board Qualification Procedure

HBM ESD tester qualification shall ensure waveform integrity of the peak current both into a short (Ips) and into a 500 ohm load as specified in Figures 2A, 2B and 3. For initial qualification, where it is possible, qualify each socket on the test fixture board.

For tester requalification, it is only necessary to use the highest pin count test fixture board with a positive clamp socket. All other positive clamp test fixture boards shall be checked when they are used in accordance with Section 8.1.2.

7.1.1 Verify electrical continuity for all pins on the test fixture board.

7.1.2 Qualification of New Test Fixture Boards

7.1.2.1 For each socket, identify the socket pin with the shortest wiring path to the pulse generation circuit. Connect this pin to Terminal B. Connect each of the other pins in turn to Terminal A. Apply a ± 1000 volt pulse using the shorting wire. All waveform parameters shall be within the limits specified in Figures 2A, and 2B, and for a 500 resistor in Figure 3.

7.1.3 Qualification of Existing Test Fixture Boards

7.1.3.1 Define the reference pin pair for each test socket on the test fixture board. Identify the socket pin with the shortest wiring path from the pulse generation circuit to the test socket. Connect this pin to Terminal B. Identify the pin with the longest wiring path from the pulse generator circuit to the ESD stress socket. Connect this pin to Terminal A.

Alternatively, the reference pin pair previously identified during MM testing may be used. (Refer to ANSI/ESD STM5.2.)

7.1.3.2 Attach the shorting wire between the reference pin pair connected to Terminal A and Terminal B. Place the current transducer around the shorting wire, as close to Terminal B as practical, observing the polarity shown in Figure 1.

- a. For positive clamp sockets, insert the shorting wire between the socket pins connected to Terminals A and B.
- b. For non-positive clamp sockets, attach the shorting wire to the wiring of the test fixture between the socket pins connected to Terminals A and B. The connection points shall be as close as possible to the test socket pins.

7.1.3.3 Apply five positive and five negative pulses. Observe waveforms at 1000 volts, 2000 volts and 4000 volts. Verify that the waveforms meet all parameters specified in Figure 2A and 2B.

7.1.3.4 Replace the shorting wire with the 500 ohm resistor. Pass the wire end of the resistor that will be connected to Terminal B through the current transducer observing the polarity shown in Figure 1.

7.1.3.5 Observe waveforms at 1000 and 4000 volts, both positive and negative polarities. Verify that the waveforms meet all parameters specified in Figure 3.

7.1.3.6 Using the shorting wire, initiate a pulse and verify that all spurious pulses are less than 15% of the amplitude of the main pulse.

NOTE 2: On analog oscilloscopes setting the time base to 1 millisecond/division can detect these types of pulses. For digital oscilloscopes, current pulses after the initial current pulse can be observed, but advanced triggering functions such as sequential triggering or delayed triggering must be applied.

7.1.3.7 If the tester has more than one pulse generation circuit, then 7.1.3.1 through 7.1.3.6 must be repeated for each independent pulse generation circuit.

7.2 Waveform Verification Procedure

Use the following procedure to verify the waveforms.

7.2.1 Verify electrical continuity for all pins on the test socket fixture board.

7.2.2 Attach the shorting wire between the reference pin pair. Place the current transducer around the shorting wire, as close to Terminal B as practical, observing the polarity shown in Figure 1.

7.2.3 Use the shorting wire to verify the waveforms at 1000 and 4000 volts (or for the stress level to be tested), for both positive and negative polarities. Verify the waveforms at 8000 volts if testing will be performed above 4000 volts. Verify that the waveforms meet all parameters specified in Figure 2A and Figures 2B.

7.2.4 Set the horizontal time scale of the oscilloscope to one millisecond per division. Initiate a pulse and verify that any spurious pulse is less than 15% of the amplitude of the main pulse.

7.2.5 If the tester has more than one pulse generation circuit, then for those pulse generation circuits used by that specific test fixture board, repeat steps 7.2.1 through 7.2.5 for each independent pulse generation circuit.

7.3 Waveform Verification following Servicing

Verify the waveforms meet all parameters specified in Figures 2A, 2B and 3 after any repairs or servicing of the tester following manufacturer's recommendations and Section 7.2.

8.0 ESDS TESTING REQUIREMENTS AND PROCEDURES

8.1 Test Requirements

8.1.1 Handling of components. Use ESD damage prevention procedures when handling components before, during and after testing.

8.1.2 Required waveform check. Verify waveform integrity (described in Section 7.2) using the shorting wire at ± 1000 volts, or the stress level to be tested. Waveform integrity shall be checked for every reference pin pair as designated in Section 7.1.3.

The waveform check is required for positive clamp sockets each time the test fixture board is changed. The waveform check is recommended for all other socket types.

Verify the waveform at least once per shift. If necessary, remove the test fixture board being used and replace with a positive clamp socket test fixture board to facilitate waveform measurements.

Longer periods between waveform checks may be used if no changes in waveforms are observed for several consecutive checks. However, if the waveforms no longer meet the specified limits, all ESD stress tests subsequent to the previous satisfactory waveform check shall be considered invalid.

If ESD stress testing is performed in consecutive shifts, waveform checks at the end of one shift may also serve as the initial check for the following shift.

If the tester has multiple pulse generation circuits, then the waveform for each pulse generation circuit must be verified with a positive clamp socket test fixture board. The time period between verification tests is once per shift. Longer periods may be used if no changes in the waveform are observed. However, if the waveform fails, then all ESD stress tests subsequent to the previous satisfactory waveform check shall be considered invalid.

8.1.3 High voltage discharge path check. Test the high voltage discharge path and all associated circuitry at the beginning of each day during which ESD stress testing is performed. Use the tester manufacturer's recommended procedure. If any failure is detected, do not perform testing with the sockets that use the defective discharge paths. Repair the tester and then verify the waveform in accordance with Section 7.3 before resuming testing.

8.1.4 Component static and dynamic tests. To determine whether components have failed, perform static and dynamic testing to all data sheet parameters before and after ESD testing. Pin leakage current may only be used as guidance in determining the component ESD withstand voltage. It is not sufficient, especially for complex integrated circuits, to use pin leakage as the only criterion for component failure.

8.1.5 Pin combinations. The pin combinations to be used for ESD stressing of all integrated circuit components are given in Table 2. Pin combination (n) is the total number of pin combinations. This varies from component to component depending on the number of power pin groups with the same name. $V_{ps(i)}$ in Table 2, is any set of like named power supply or ground pins (e.g., Vcc, Vss, Vdd, analog GND, digital GND, etc.) which are metallurgically connected (within 3 ohm) on the chip or within the package. Like named pins that are resistively connected via the chip substrate or wells, or are electrically isolated from each other (more than 3 ohms), are considered separate sets for the purpose of these tests. For example, if two pins are labeled Vcc, but are not metallurgically connected and the resistance is greater than 3 ohms within the chip/package, then they shall be treated as distinct and separate $V_{ps(i)}$ sets. Only those pins that supply current to or interface to other pins shall be considered to be power pins. Pins such as Vcc, Vdd, GND, Vss, Vee, +Vs and -Vs are considered power supply pins. These pins supply current to input and output buffers in such a way as to interface closely with the environment through other pins.

Pins such as offset adjust, compensation, clocks, controls, address, data, Vref, output and input pins are considered non-power supply pins. For example, a programming power pin, usually called Vpp, shall be considered to be a non-power supply pin because it does not supply current to or interface with any other pins.

No connect pins will not be HBM stressed.

For further clarification on pin combinations, see example in Annex A.

Table 2. Pin Combinations for all Digital, Analog and Hybrid Integrated Circuits

Pin Combination Set	Connect Individually to Terminal A	Connect to Terminal B (Ground)	Floating Pins (Unconnected)
1	All pins one at a time, except the pin(s) connected to Terminal B	Vps(1) [First power pin(s)]	All pins except pin under test (PUT) and Vps(1) [First power pin]
2	All pins one at a time, except the pin(s) connected to Terminal B	Vps(2) [Second power pin(s)]	All pins except PUT and VPS(2) [Second power pin]
(i)	All pins one at a time, except the pin(s) connected to Terminal B	Vps(i) [ith power pin(s)] [1,2, ... i]	All pins except PUT and Vps(i)
n-1	All pins one at a time, except the pin(s) connected to Terminal B	Vps(n-1)	All pins except PUT and Vps(n-1)
n	All non-Vps(i) pins one at a time.	All other non-Vps(i) pins, except the pin connected to Terminal A	All Vps(i) pins and redundant Shorted I/O Pins

Pin combinations to be used for ESD stressing of all active and passive discrete components and component arrays are given in Section 8.1.5.1.

8.1.5.1 Pin combinations for all discrete components and component arrays (including both passive and active components) shall be HBM stressed as follows:

All possible pin pair combinations (one pin to Terminal A, another to Terminal B), regardless of pin function, shall be used for discrete components.

8.1.5.2 For non-supply pins that are metallurgically connected on the chip or within the package, when any one of these pins is stressed (Terminal A), the remainder of these pins (Shorted I/O pins) shall be left floating and all other non-supply pins shall be held at ground (Terminal B).

8.2 HBM Classification and ESD Stress Testing Procedure

Classify components according to their HBM ESD withstand voltage. Perform ESD stress testing at room temperature in accordance with the procedure below. It is permissible to use any voltage level in Table 3 as the starting stress level. Three new components may be used at each voltage level or pin combination if desired. This will eliminate any step stress hardening effects, and reduce the possibility of early failure due to cumulative stress on power pins. However, if a single set of three components is stressed at each level, then to avoid missing possible ESD vulnerability windows, it is recommended not to miss any stress step.

ESD classification testing shall be considered destructive to the component, even if no component failure occurs.

Table 3. HBM ESD Stress Levels

Stress Level	Equivalent Charging (\pm) voltage Vp (volt)
1	250
2	500
3	1000
4	2000
5	4000
6	8000 (optional)

NOTE 3: A component may pass at 4000 volts but fail at 2000 volts; this is called a component fail window. To avoid this fail window, it is recommended that components are tested at each classification level defined in Table 3.

Use the following procedure to classify components:

8.2.1 Test a minimum of three samples of the component to all specified static and dynamic data sheet parameters.

8.2.2 Determine the starting stress voltage level from Table 3. Select the first pin combination to be tested as stated in Section 8.1.5.

8.2.3 Apply one positive and one negative pulse to the component. Allow at least a 0.3 second interval between pulses. Repeat this process using all other pin combinations specified in Section 8.1.5.

8.2.4 Test the components to full static and dynamic data sheet parameters and record the results for each component. Parametric and functional testing shall be performed at room temperature. If testing is required at multiple temperatures, testing shall be performed at the lowest temperature first.

If all three components pass the specified data sheet parameters, repeat steps 8.2.3 through 8.2.4, using the next higher stress level of Table 3. Three new components may be used at each voltage level or pin combination if desired.

8.2.5 If one or more components fail, repeat the ESD stress test using three new components starting at the next lower stress level. If the components continue to fail, decrease the stress voltage until level 1 is reached in Table 3. If any additional failures are observed at level 1, stop all testing at this level.

NOTE 4: In Annex B, the HBM Test Procedure Flow diagram has been added so that the user can review an outline of the test steps required from equipment qualification to component level classification.

9.0 FAILURE CRITERIA

A component is considered an ESD failure if it fails the data sheet parameters as specified in Section 8.2.4.

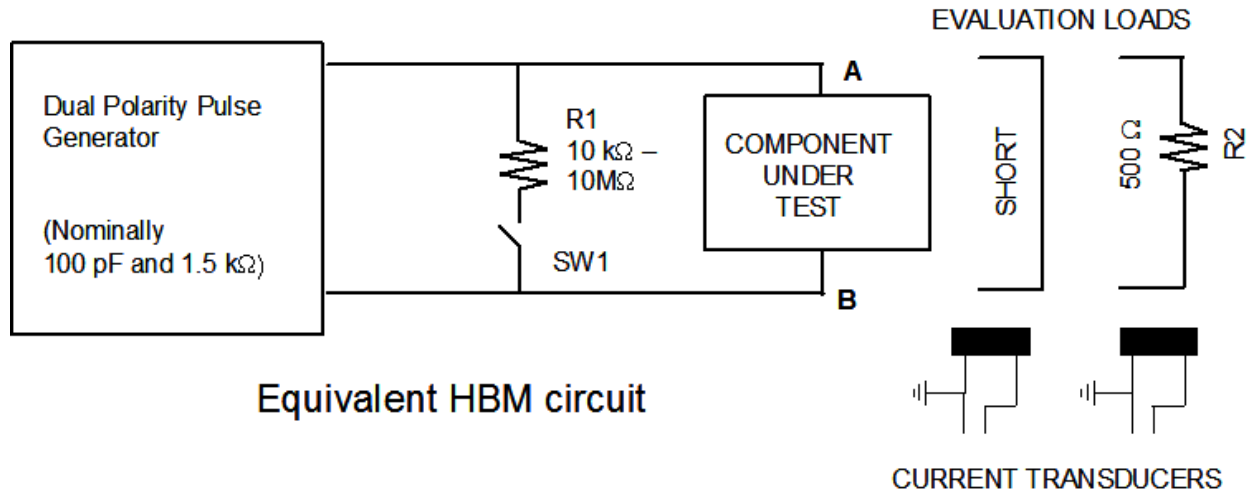


Figure 1: HBM Simulator's Schematic with Evaluation Loads

Requirements:

1. The current transducers are specified in 5.2.3.
2. The shorting wire and 500 ohm resistor R2 are specified in 5.2.2.
3. Reversal of Terminals A and B to achieve dual polarity performance is not permitted.
4. SW1 is closed 10 to 100 milliseconds after the pulse delivery period to ensure the socket is not left in a charged state. The switch should remain closed for at least 5 milliseconds and it should be opened at least 10 milliseconds prior to the delivery of the next pulse. The resistance R1 in series with the switch ensures a slow discharge of the device, thus avoiding the possibility of a charged device model discharge.
5. The Dual Polarity Pulse Generator shall be designed to avoid recharge transients and double pulses.
6. Piggybacking of test sockets (the insertion of secondary sockets into the main test socket) is allowed only if the secondary socket waveform meets the requirements of this standard.
7. Measure the current waveform as described in Section 7.2.

NOTE 5: Devices under test with very high impedance will develop a voltage between terminals A and B in the tens to hundreds of microseconds before the HBM current pulse. This voltage is the result of redistribution of charge between the 100 picofarad capacitor and other parts of the system as the relay that initiates the current pulse closes and the relay capacitance changes. The voltage prior to the current pulse is not an HBM simulator artifact, but is present in real human body ESD events. A procedure for measuring this voltage is given in Annex D. The pre-current pulse voltage between Terminals A and B has been shown to cause some ESD protection circuits not to perform as expected. Dynamically triggered clamps are the most sensitive to this voltage.

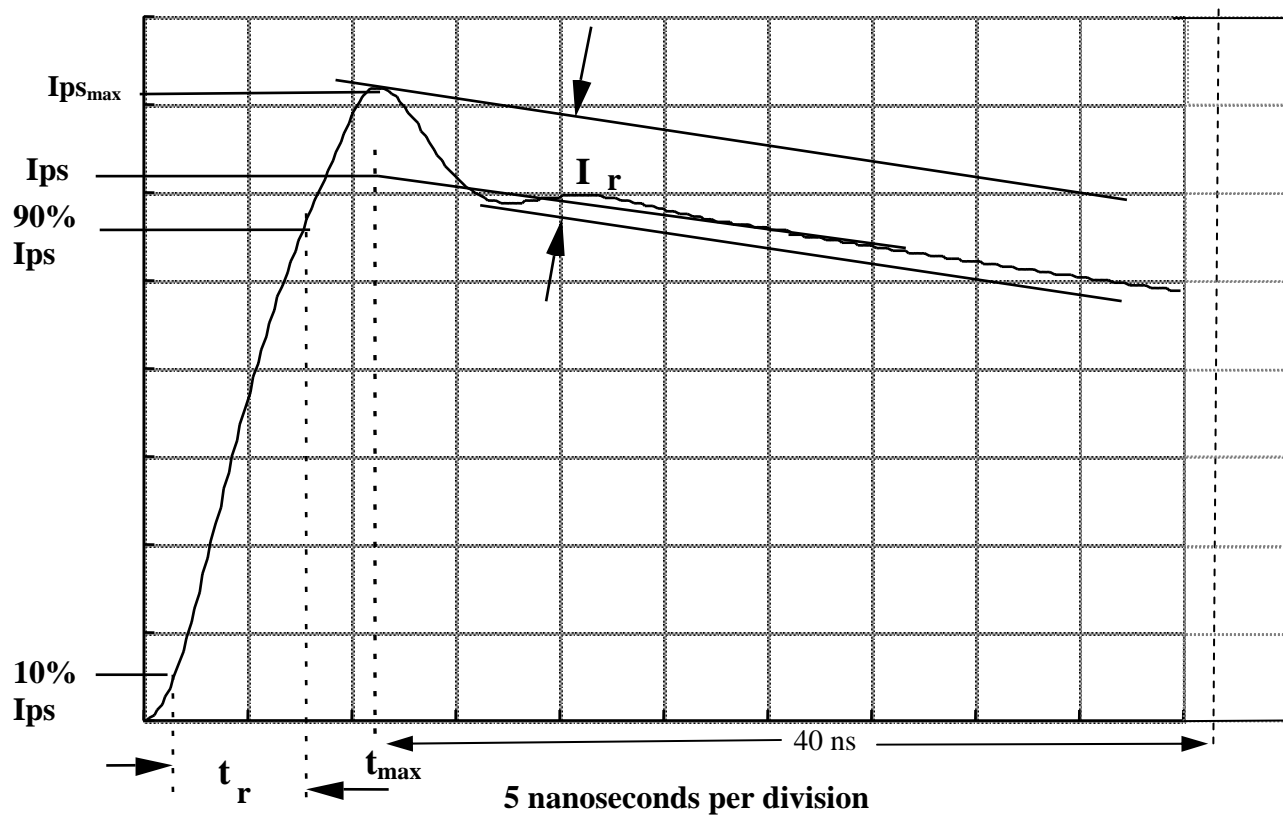


Figure 2A: Current Waveform through a Shorting Wire ($I_{ps_{max}}$)

Table 4. HBM Stress Voltages and Ips Values

Equivalent Charging (\pm) voltage V_p (volt)	Ips (Ampere)
250	0.17 ($\pm 10\%$)
500	0.33 ($\pm 10\%$)
1000	0.67 ($\pm 10\%$)
2000	1.33 ($\pm 10\%$)
4000	2.67 ($\pm 10\%$)
8000 ^a	5.33 ($\pm 10\%$)

^a Optional, only needed if testing performed above 4000 volts.

Table 5. Pulse Rise Time and Peak to Peak Ringing

Parameter	Value
t_r (pulse rise time)	2 to 10 nanoseconds
I_r (peak to peak ringing)	< 15% of Ips. No ringing 100 nanoseconds after start of pulse

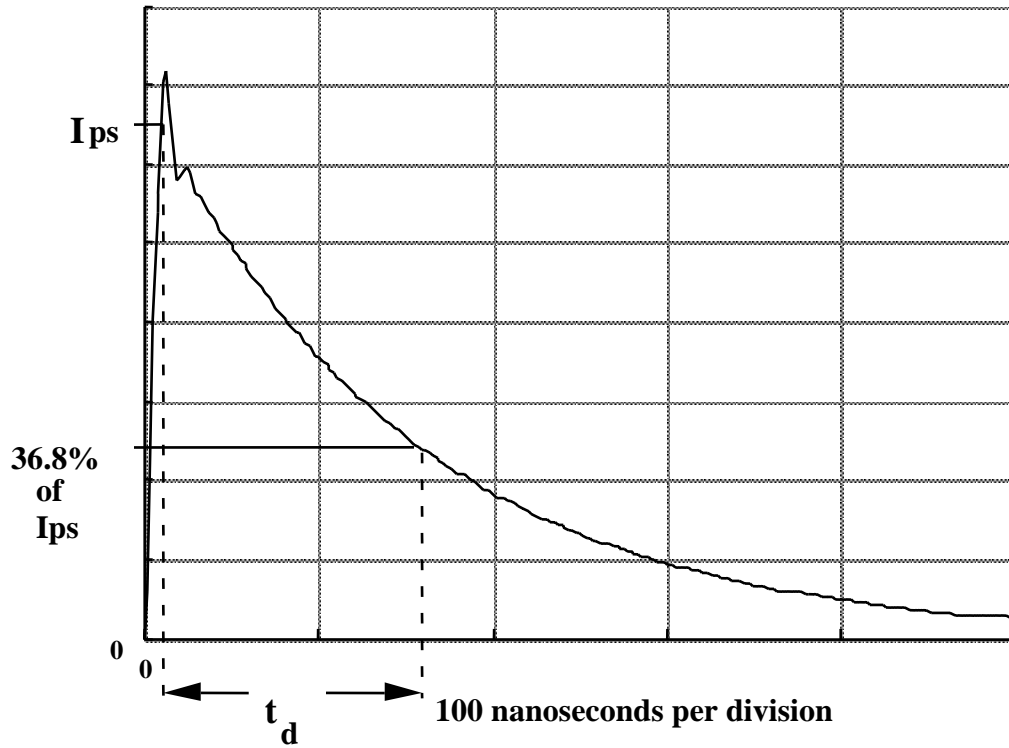


Figure 2B: Current Waveform through a Shorting Wire (t_d)

Table 6. I_{ps} Discharge Current Pulse Duration (t_d)

Parameter	Value
t_d (pulse duration)	150 nanoseconds \pm 20 nanoseconds

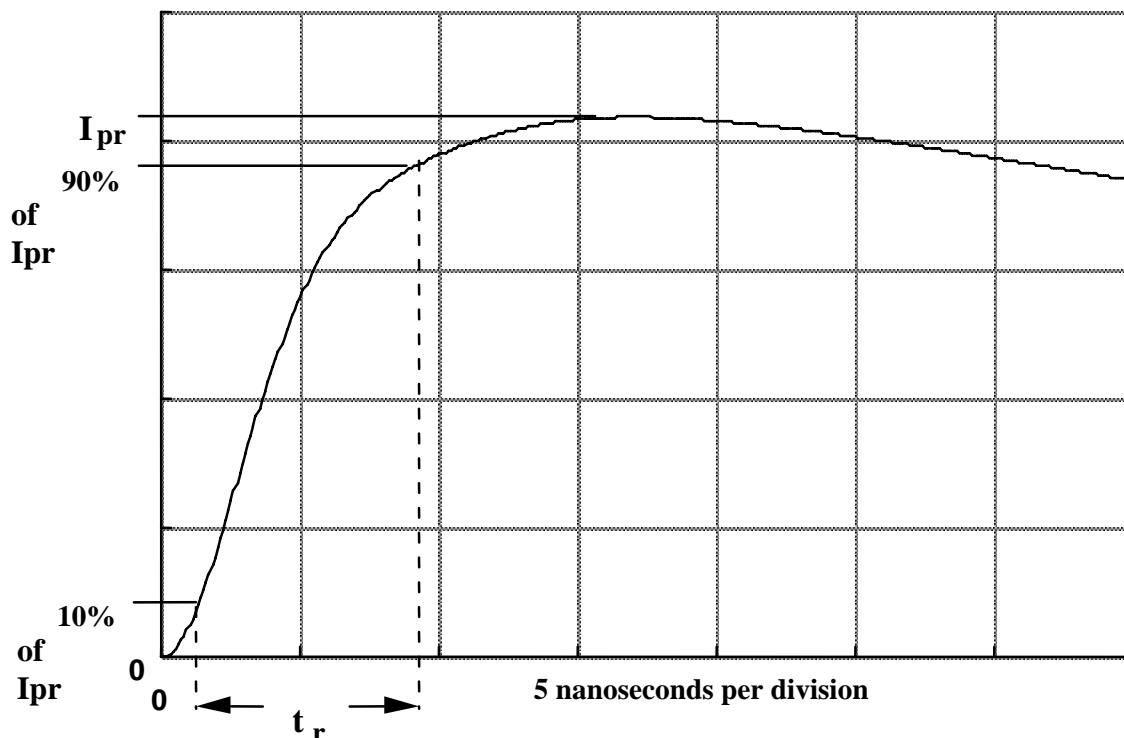


Figure 3: Current Waveform through a 500 ohm Resistor

Table 7. 500 ohm Load Ipr Values

Parameter	500 ohm Load Values
I_{PR}	375 – 550 milliamperes for 1000 volt pre-charge
I_{PR}	1.5 – 2.2 A for 4000 volt pre-charge
I_{PR}/I_{PS}	$\geq 63\%$

Requirement:

8. The current pulse shall meet the following characteristics:

t_r Pulse rise time 5 nanoseconds to 25 nanoseconds.

I_r The maximum allowable peak-to-peak ringing must be less than 15% of I_{pr} , when measured parallel to the current waveform, with no observable ringing 100 nanoseconds after the start of the pulse.

NOTE 6:

The peak current and risetime into the 500 ohm resistor will vary, depending upon the capacitive loading of the socket and peripheral wiring. It is not necessary to measure t_d , pulse decay time of the current through the 500 ohm resistor, as this will vary, depending upon how the tester forms the pulse. The 500 ohm waveform standard is intended to assure that socket capacitance is limited. But for a given component, socket capacitance within those limits could still influence ESD withstand voltage.

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ANNEX A (INFORMATIVE)

Example of pin combinations using Table 2.

The following example is intended to clarify the pin combinations given in Table 2. The example is for a 10 pin device with 2-Vdd, 2-Vss, 2-Vcc, 2-input and 2-output pins. It is assumed that the like-named power supply pins are metalically connected. If not, each should be treated as an individual supply pin.

Example of Pin Combinations

Sequence Number	Pin Combination	Connect to A	Connect to B	Float Pins
1	1	1st input pin	2-Vdd	all other 7 pins
2	1	2nd input pin	2-Vdd	all other 7 pins
3	1	1st output pin	2-Vdd	all other 7 pins
4	1	2nd output pin	2-Vdd	all other 7 pins
5	1	1st Vcc pin	2-Vdd	all other 7 pins
6	1	2nd Vcc pin	2-Vdd	all other 7 pins
7	1	1st Vss pin	2-Vdd	all other 7 pins
8	1	2nd Vss pin	2-Vdd	all other 7 pins
9–12	2	Repeat 1–4	2-Vss	all other 7 pins
13	2	1st Vcc pin	2-Vss	all other 7 pins
14	2	2nd Vcc pin	2-Vss	all other 7 pins
15	2	1st Vdd pin	2-Vss	all other 7 pins
16	2	2nd Vdd pin	2-Vss	all other 7 pins
17–20	3	Repeat 1–4	2-Vcc	all other 7 pins
21	3	1st Vss pin	2-Vcc	all other 7 pins
22	3	2nd Vss pin	2-Vcc	all other 7 pins
23	3	1st Vdd pin	2-Vcc	all other 7 pins

Example of Pin Combinations (continued)

Sequence Number	Pin Combination	Connect to A	Connect to B	Float Pins
24	3	2nd Vdd pin	2-Vcc	all other 7 pins
25	4	1st input pin	outputs 1, 2 & input 2	all Vdd, Vss & Vcc pins
26	4	2nd input pin	outputs 1, 2 & input 1	all Vdd, Vss & Vcc pins
27	4	1st output pin	inputs 1, 2 & output 2	all Vdd, Vss & Vcc pins
28	4	2nd output pin	inputs 1, 2 & output 1	all Vdd, Vss & Vcc pins

NOTE A1:

Power supply and ground pins include Vdd, Vcc, Vss, GND, Grd, +Vs, -Vs, etc. as defined in Section 8.1.5. Pins such as offset adjust, compensation, clocks, controls, address, data and input shall be considered non-power supply pins. For each combination sequence, follow the procedure established in Section 8.2.

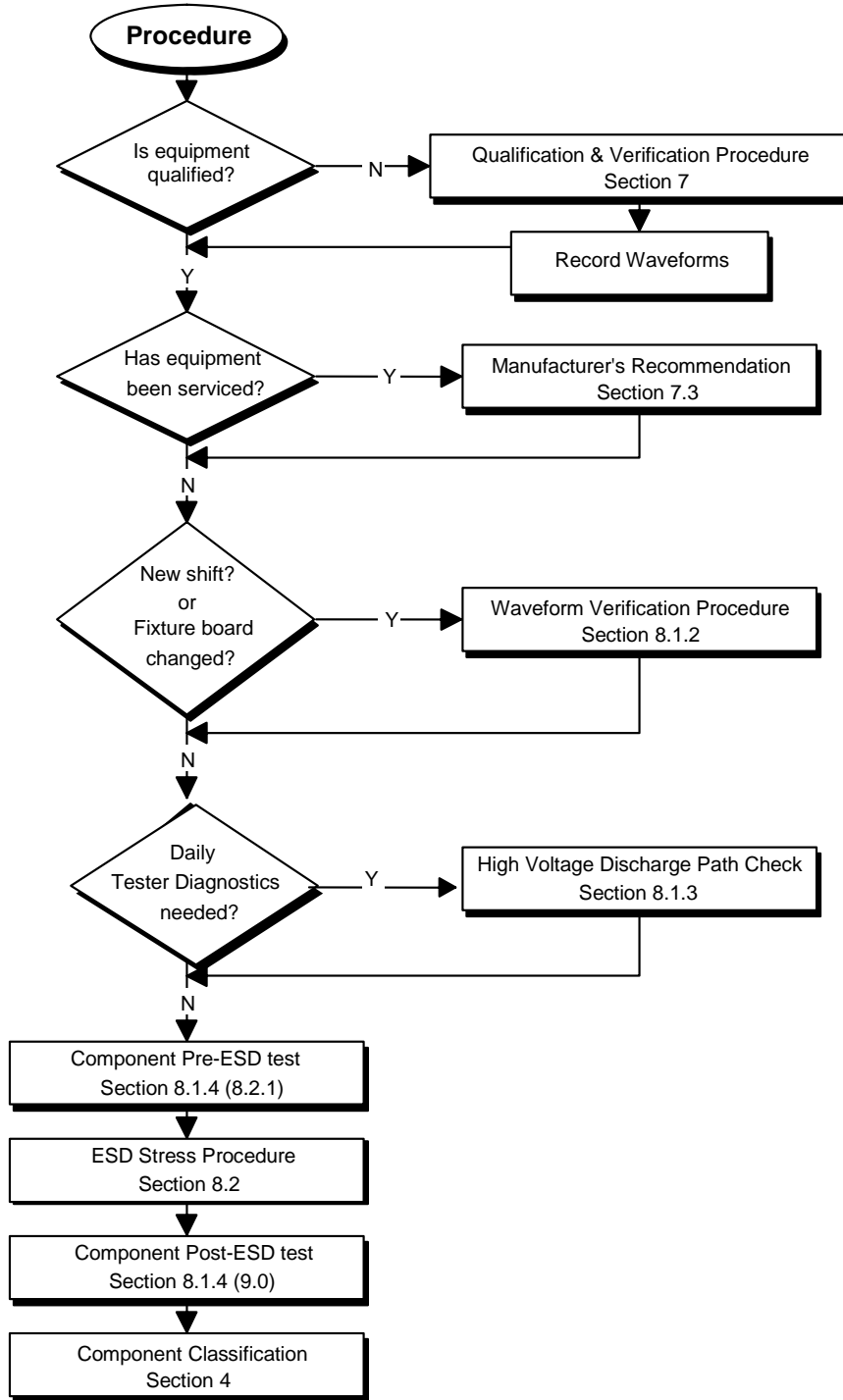
The sequence number refers to the sequence of pin combinations for stressing.

NOTE A2:

Due to equipment limitations, the HBM stressing of no connect (NC) pins has been removed from the pin combinations. These pins should not be HBM stressed at this time.

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ANNEX B (INFORMATIVE)
HBM STM5.1 Procedure Flow



(This annex is not part of ANSI/ESD STM5.1-2007)

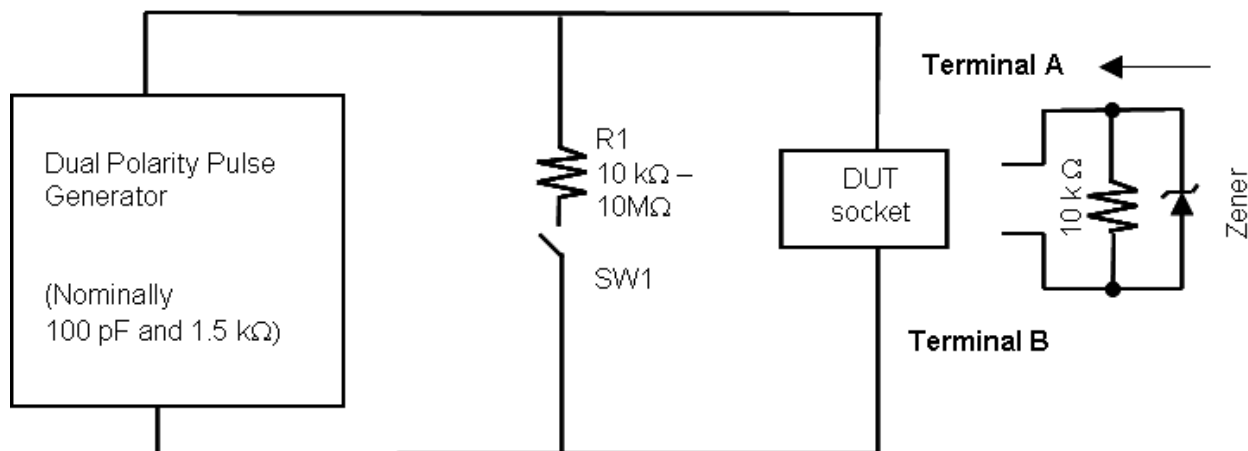
ANNEX C (INFORMATIVE)**C1. Trailing Current Pulse Measurement Setup**

Figure 4: Diagram Illustrates the Schematics of Trailing Pulse Measurement Setup

Research has demonstrated that HBM sensitivity levels can be falsely classified due to the parasitic artifacts unintentionally built into the HBM simulators. This issue may or may not be present in an ESD simulator. To determine if the “Trailing Current Pulse” parasitic artifact is present, the following measurements should be performed.

A circuit for measuring the trailing current pulse is shown in Figure 4. The voltage probe shall have input impedance no less than 10 megohm, an input capacitance no larger than 10 picofarad, a bandwidth better than 1 megahertz, and a voltage rating to withstand at least 15 volts. The resistance is 10 kilohm in value with tolerance of +/- 1% and can withstand up to 4000 volts. The Zener diode has a breakdown voltage range from 6 to 15 volts and a power rating values from ¼ to 1 watt.

C2. Measurement Procedure

- C2.1 The trailing current pulse measurement shall be done with an ESD fixture (e.g. DIP socket) installed and with no part in the socket.
- C2.2 Connect the load resistor in parallel with the Zener diode, between terminal A and terminal B of the DUT socket as shown in the Figure 4.
- C2.3 Connect the voltage probe to monitor the trailing pulse waveform across the load resistor. Adjust the scope input impedance to 1 megaohm, if the scope does not do it automatically.
- C2.4 Adjust the scope settings to 200 microsecond and 20 millivolt per division. If waveform is not detected, then adjust the scope setting to lower time scales.
- C2.5 Adjust the trigger level on the scope and put on ready.
- C2.6 Initiate an ESD pulse at positive 4000 volts (Figure 5A).
- C2.7 Repeat the waveform measurement at negative 4000 volts (Figure 5B).
- C2.8 Both waveforms in steps C2.6 and C2.7 shall meet the requirement as specified in Section 5.

NOTE C1: If the waveform goes off scale, use a larger scale (more than 20 millivolt per division) in order to determine the trailing pulse level.

NOTE C2: It is recommended to make use of 20 megahertz bandwidth limitation and/or multiple pulse averaging, if the scope allows, to reduce the noise.

C3. Typical Examples of Trailing Pulse Waveform

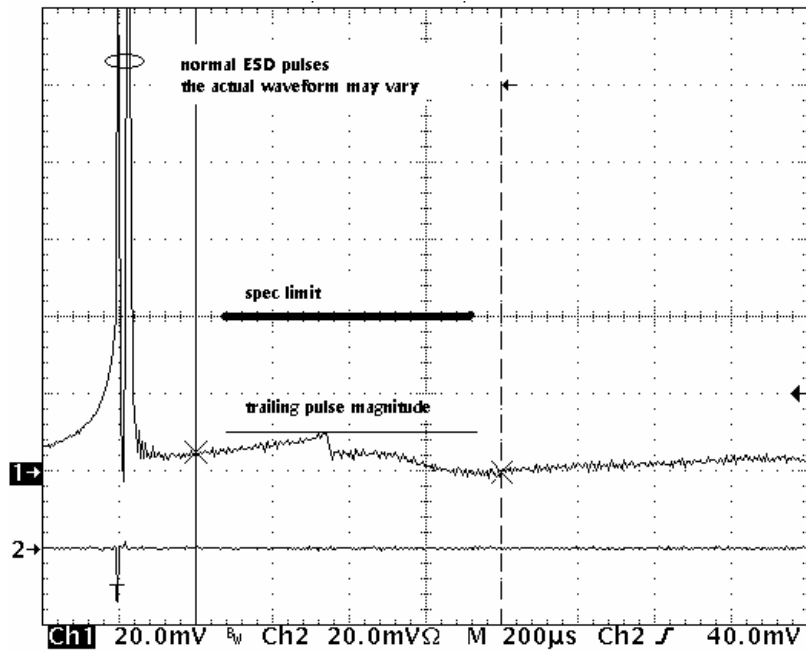


Figure 5A: Positive Stress at 4000 Volts

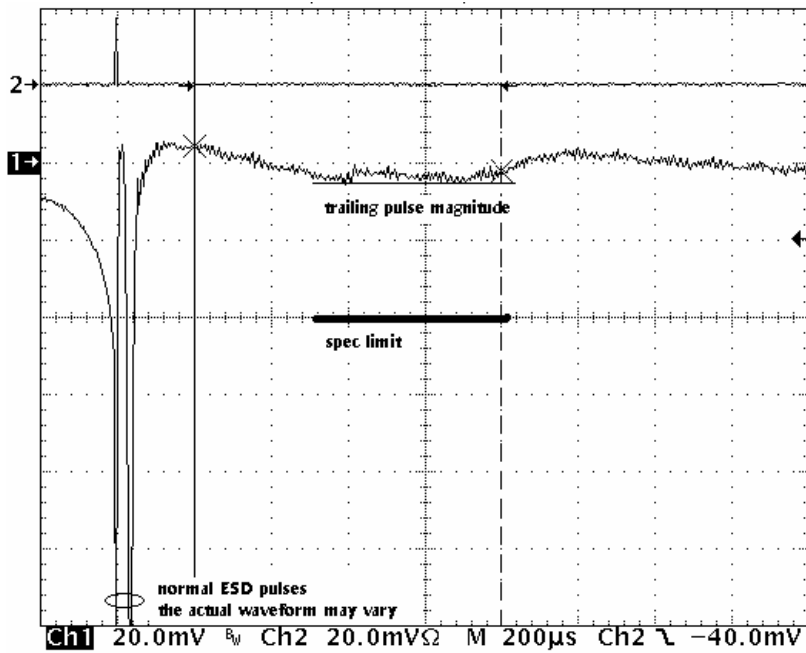


Figure 5B: Negative Stress at 4000 Volts

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ANNEX D (INFORMATIVE)

A circuit for measuring the voltage before the HBM current pulse is shown in Figure 6A.

D1. Voltage before the HBM Current Pulse Measurement Setup

The worst-case condition will be measured for a low capacitance Zener diode with a voltage in the 8 to 10 volt range. The Zener diode will provide protection for the voltage probe and its low capacitance will not reduce the voltage buildup appreciably. The current transducer on the groundside of the diode is used to trigger an oscilloscope. The voltage probe, connected to a second channel of the oscilloscope, should have high resistance such as a 10 megohm 10X probe. Sample data is shown in Figure 6B for a 9.4 volt Zener diode. The HBM current pulse occurs at time zero and cannot be seen at this time scale. At the time scale of an HBM event, tens to hundreds of nanoseconds, the voltage before the HBM current pulse would appear as a DC voltage across the diode. To measure the voltage across a device the Zener diode is replaced by the device of interest.

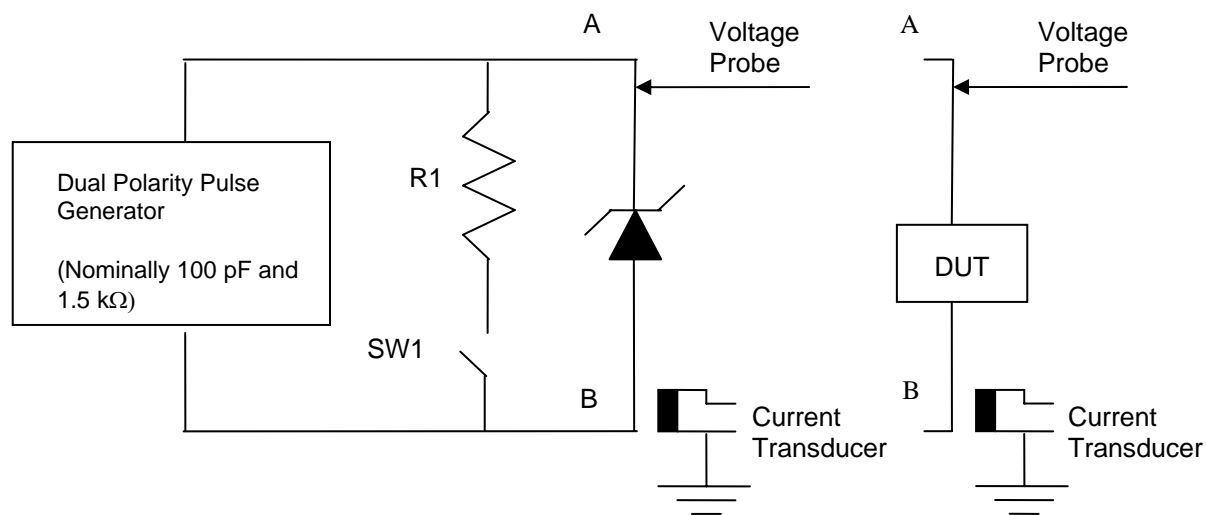


Figure 6A: Circuit for Measuring Voltage before Current Pulse on a Zener Diode or on a Device

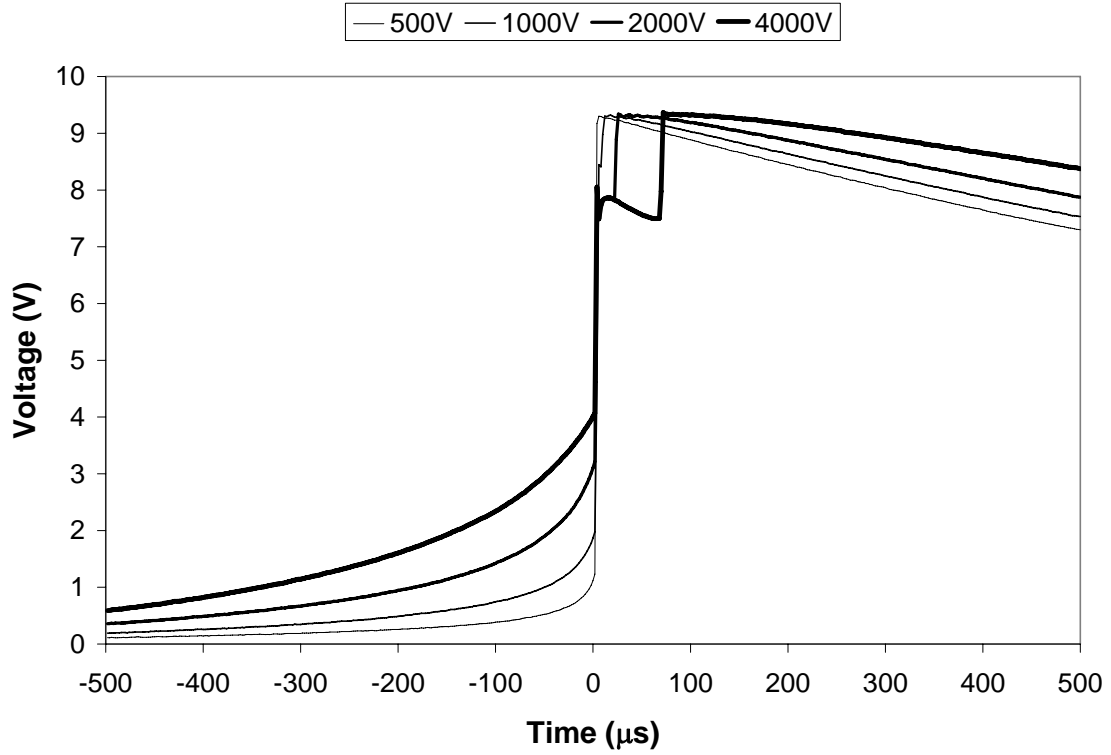


Figure 6B: Example Voltage Rise before the HBM Current Pulse across a 9.4 volt Zener Diode

The current pulse occurs at time 0.

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ANNEX E (INFORMATIVE)

Bibliography

MIL-STD-883D: Test Methods and Procedures for Microelectronics: Method 3015.7 Electrostatic Discharge Sensitivity Classification.

MIL-STD-750C Notice 4: Test Methods for Semiconductor Devices: Method 1020: Electrostatic Discharge Sensitivity Classification.

(This annex is not part of ANSI/ESD STM5.1-2007)

ANNEX F (INFORMATIVE)

ANSI/ESD STM5.1-2007 Revision History

1. New HBM definitions added: Component; Discrete component; $I_{ps_{max}}$; t_{max} ; I_{ps} ; Spurious current pulses; Trailing current pulse; Shorted I/O pin; No Connect (NC) pin; Pulse Generation Circuit; Voltage before the HBM Current Pulse; I_r ; New equipment; and Old equipment.
2. Equipment and waveform requirements changes:
 - a. Section 6.3.1 - Specifically requested that waveforms from short circuit and 500 ohm load resistor be recorded. Deleted wording on saving as photographs or digitized waveforms. Wording slight re-edited.
 - b. Section 6.3.2 – Slight change – a sentence from 6.3.1 was moved into 6.3.2.
 - c. Section 6.4 Trailing Current Pulse Check (Optional) was added.
3. Qualification and Verification procedure updates:
 - a. Section 7.1 – slight edit of procedure – limited the requirement that each test socket must have the short circuit and 500 ohm current waveforms recorded. In some cases this waveform measurement cannot be made due to the construction of the socket. The updated procedure limits this requirement to those sockets that can physically be measured with a short and 500 ohm resistor.
 - b. Addition of a new Note 2 after 7.1.3.6. Comments regarding detection of HBM pulse using analog versus digital scopes.
 - c. New Section 7.1.3.7 was added to account for the new HBM simulators that use multiple generation circuits.
 - d. Section 7.2.5 was added to account for the new HBM simulators that use multiple generation circuits.
4. Waveform verification following service changes:
 - a. Section 7.3 was added to insure that after servicing, the waveforms of the ESD simulator still meet the short and 500 ohm requirements.

ESDS testing requirements and procedures 8 updates:

- b. Section 8.1.2 was modified to account for new HBM simulators that use multiple generation circuits.
 - c. Section 8.1.3 wording was slightly modified to improve the readability.
 - d. Section 8.1.4 wording was slightly modified to improve the readability.
 - e. Section 8.1.5 Pin Combinations has been changed. The edits relax the definition of the bus resistance between like name power pins from 2 ohm to 3 ohm, the NC (No connect) pin test was removed,
 - f. Section 8.1.5.1 wording was simplified.
 - g. Section 8.5.1.2 was added to include Shorted I/O pins. This is a new type of pin where two pins are shorted together in the package.
 - h. Section 8.1.5.1 and 8.5.1.2 were moved and placed after Table 2.
 - i. Table 2 was modified under Pin Combination “n” – Column under Floating Pins was modified to include Shorted I/O Pins.
5. Figure 1 edits:
 - a. The caption under Figure 1 was improved.
 - b. Requirement 4 was reworded to be more specific on the operation of SW1.
 - c. Note 5 is now new as this introduces the idea of HBM voltage at the DUT prior to current pulse
 6. Figure 2A edits:
 - a. The maximum peak current is now defined as $I_{ps_{max}}$.
 - b. The time where $I_{ps_{max}}$ occurs is now defined at t_{max} .
 - c. The time for extrapolating a straight line along the exponential decay is defined as 40 ns.
 7. Figure 3 edits:
 - a. The table below Figure 3 title was changed to 500 ohm Load Values from Values.
 - b. The units under Parameter were removed; since they were defined under the 500 ohm Values column.
 - c. Require I_{pr} was deleted as this statement was redundant to information in the table.
 8. Annex A was changed to include additional pin combinations possible for this simple example.
 - a. Note A2 was added to state that No Connect (NC) pins will no longer be HBM stressed.
 9. Annex C procedure was added to clearly define how to measure the Trailing Current Pulse. This is a new optional test equipment requirement.
 10. Annex D procedure was added to show how to correctly measure the Voltage before the HBM Current Pulse.